Starter

In your group, decide on your roles below. Then look at the instructions document for your role – do not look at the others!

- CPU
- Display
- Main memory
- AU (for groups of 4 only)

Extension:
Estimate your group's average clock speed

Processors 1

Specification

4.7.3.1 The processor and its components

Content

Explain the role and operation of a processor and its major components:

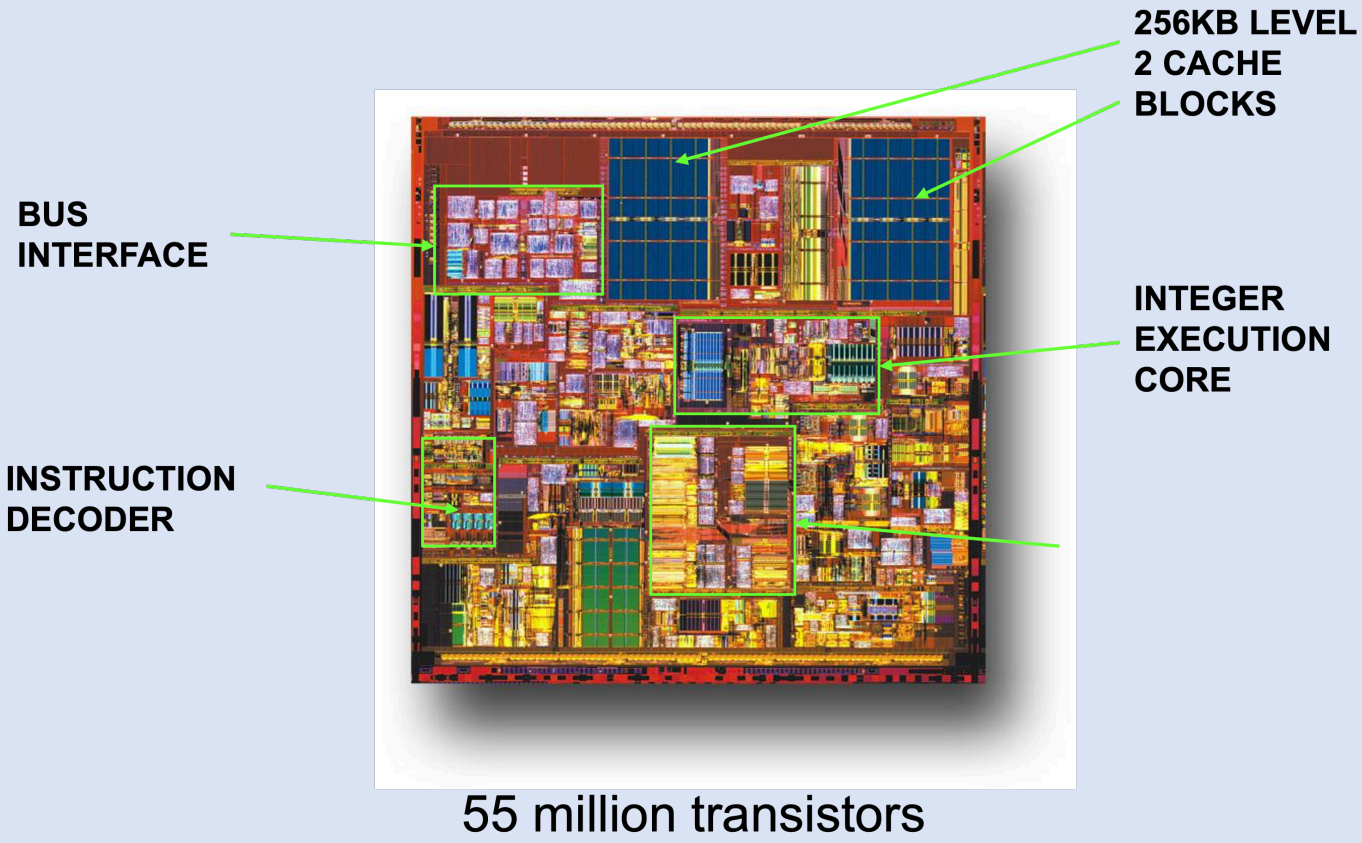
- arithmetic logic unit
- control unit
- clock
- general-purpose registers
- dedicated registers, including:
  - program counter
  - current instruction register
  - memory address register
  - memory buffer register
  - status register.

4.7.3.2 The Fetch-Execute cycle and the role of registers within it

Content

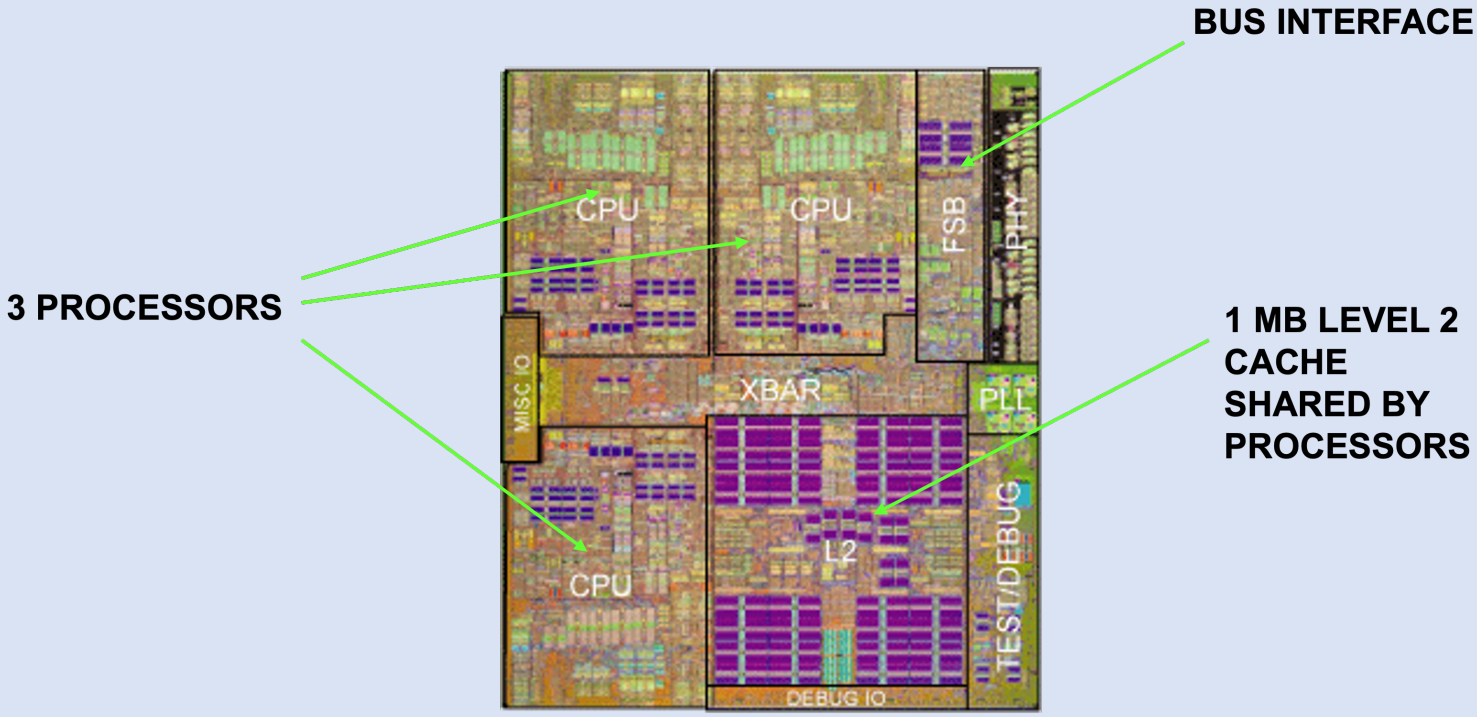
Explain how the Fetch-Execute cycle is used to execute machine code programs including the stages in the cycle (fetch, decode, execute) and details of registers used.

Pentium 4 Processor



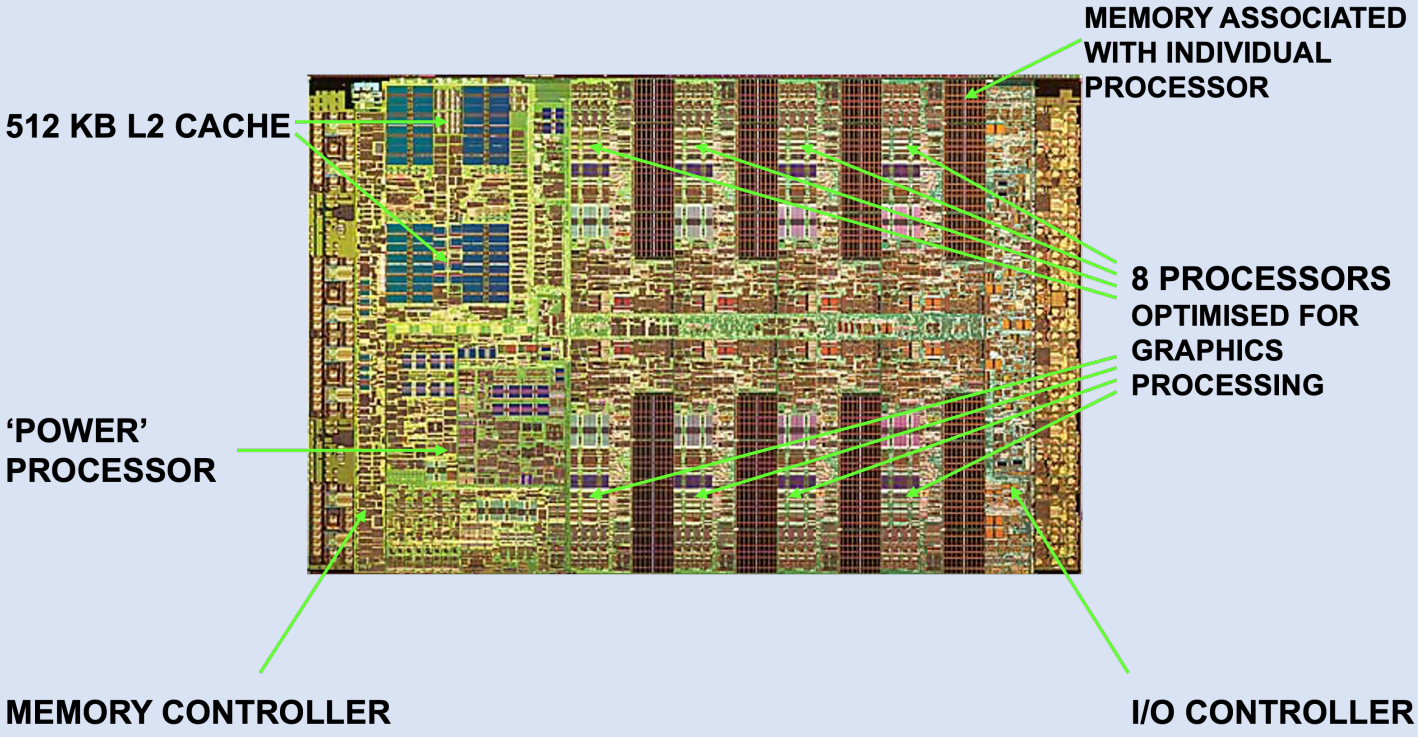
55 million transistors

Xbox 360 Processor



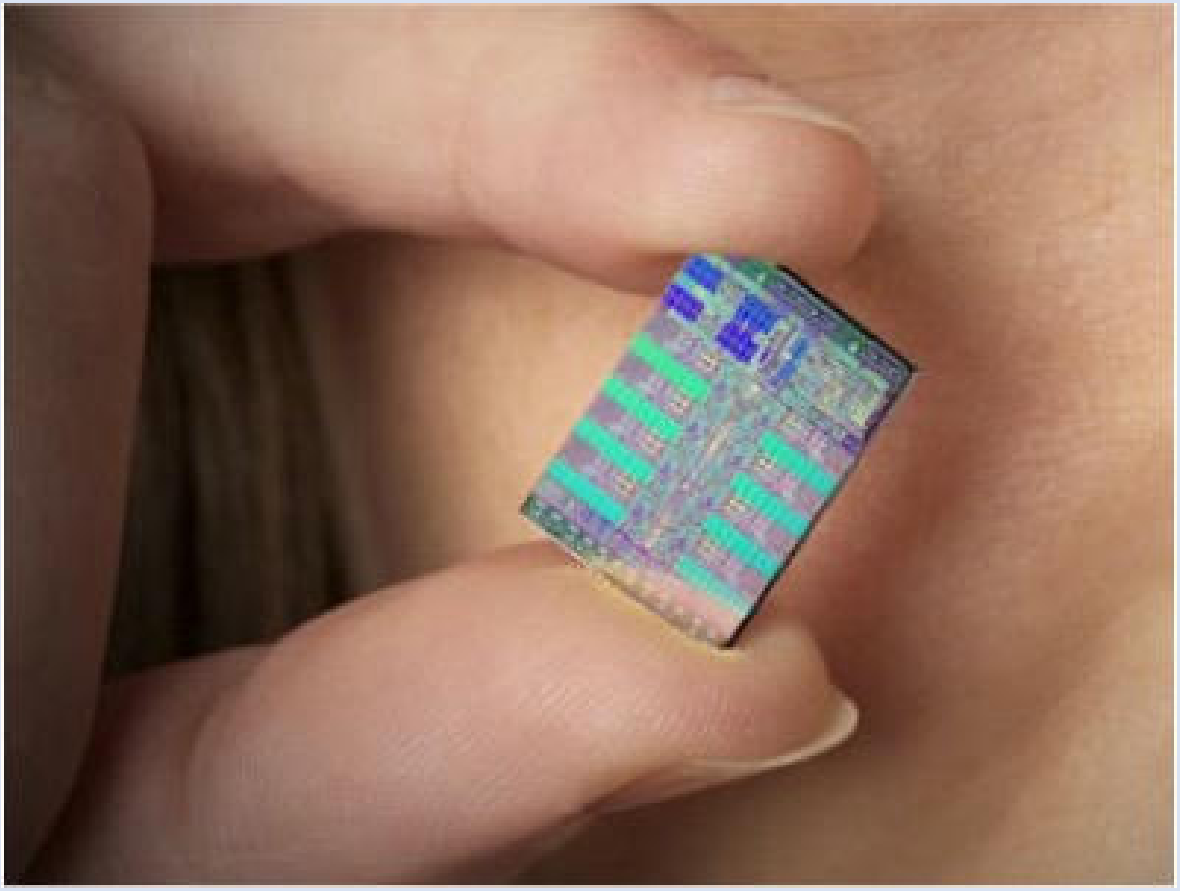
165 million transistors

PlayStation 3 Processor



234 million transistors

PlayStation 3 Processor



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- **Internal buses & logic gates**

The role of the control unit

To marshal / control operation of fetch-execute cycle;
Controls fetching / loading / storing operations; **N.E.** fetches instructions
Determines the type of an instruction; **A.** decodes instructions
To execute (some) instructions;
To synchronise operation of processor;
To send control signals / commands to other components;
To control the transfer of data between registers;
To handle interrupts;

This is the mark scheme for a past exam question:

Describe the role of the control unit

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What is the stored program concept?

- A program's instructions must be resident in main memory for it to be executed
- Instructions are fetched and executed one at a time by the processor

Let's see how that second point happens...

Fetch-decode-execute cycle (GCSE)

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This sequence is repeated for each instruction.

Processor instructions

- Instructions do not look like the code we have been writing so far (e.g. C#)
- Each instruction consists of an **opcode** and zero or more **operands**
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- `ADD` is the opcode
- `R1` and `#15` are operands

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  - Most Windows machines are based on the x86 instruction set architecture
    - Intel
    - AMD
  - ARM is on the rise – it has excellent power efficiency
    - Raspberry Pi
    - Apple Silicon (M1-M4, A4-A18 etc.)
    - Snapdragon

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- Small blocks of memory on the processor itself
  - Incredibly fast, because it’s directly on the processor
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- Some are general-purpose
  - Used within machine code for temporary storage
- Some are dedicated registers, used for the operation of the computer itself

MAR & MBR

- **Memory address register (MAR)**
  - Holds the **address** of a memory location from which data will be read from or written to
  - Processor's direct connection to the **address bus** for accessing main memory
  - Can hold the address of the next instruction to be fetched, or the address of data to be used in an instruction

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- **Memory buffer register (MBR)**
  - Temporarily stores **data** read from or to be written to memory
  - Processor's direct connection to the **data bus** for accessing main memory
  - Can hold the next instruction to be executed or data to be used in an instruction

Program counter (PC)

- Holds the address of the next instruction to be executed
- Incremented as part of the fetch-decode-execute cycle

Current instruction register (CIR)

- Stores the current instruction in binary
- The “decode” step is performed on the CIR

Status register (SR)

- Each bit corresponds to a particular status value
  - Overflow
  - Negative result
  - Zero result
  - …
- Each bit is set (`1`) or cleared (`0`) depending on the result of the operation

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  7. The instruction held in the **CIR** is decode by the **control unit** into **opcode** and **operands**

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Ada Quiz: L106 - Processors 1